1. (AMENDED) An apparatus comprising:

a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain configured to receive said first supply voltage, and (iii) a first source coupled to a first output; and

a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said second supply voltage, wherein said apparatus is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage.

2. (AMENDED) The apparatus according to claim 1, wherein said input voltage ranges up to twice said first supply voltage with respect to said second supply voltage.

3. (AMENDED) The apparatus according to claim 1, wherein said first device is configured in a source-follow configuration.

4. (AMENDED) The apparatus according to claim 1, wherein said first device comprises an NMOS device.

103 5. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a native NMOS device.

103 7. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a PMOS device.

(Continued)

103 8. (AMENDED) The apparatus according to claim 1, wherein said first device comprises a native PMOS device.

misdescription 103 9. The apparatus according to claim 1, wherein said first supply voltage comprises a ground voltage.

102 10. The apparatus according to claim 1, wherein said second supply voltage comprises a ground voltage.

102 11. (AMENDED) A method for implementing voltage protection comprising the steps of:

configuring a device to have (i) a gate for receiving an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a drain for receiving said first supply voltage, and (iii) a source coupled to an output; and

configuring a resistive element to have (i) a first side coupled to said source and (ii) a second side for receiving said second supply voltage, wherein said device and said resistive

element are arranged such that a maximum voltage drop across a gate oxide of said device does not exceed a difference between said first supply voltage and said second supply voltage.

12. (AMENDED) The method according to claim 11, wherein said input voltage ranges up to twice said first supply voltage with respect to said second supply voltage.

13. The method according to claim 11, wherein said device is configured in a source-follow configuration.

14. The method according to claim 11, wherein said device comprises an NMOS device.

15. The method according to claim 11, wherein said device comprises a PMOS device.

16. The method according to claim 11, wherein said device comprises a native NMOS device.

17. The method according to claim 11, wherein said device comprises a native PMOS device.

18. (AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain configured to receive said second supply voltage, and (iii) a first source coupled to a first output, and (B) a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said first supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate coupled to said first output, (ii) a second drain configured to receive said first supply voltage, and (iii) a second source coupled to a second output, and (B) a second resistive element having (i) a first side coupled to said second source and (ii) a second side configured to receive said second supply voltage, wherein said apparatus is arranged such that a maximum voltage drop across a gate oxide of said first device does not exceed a difference between said first supply voltage and said second supply voltage.

19. The apparatus according to claim 1, further comprising:

a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain configured to

receive said second supply voltage, and (iii) a second source coupled to a second output;

a second resistive element having (i) a first side coupled to said second source and (ii) a second side configured to receive said first supply voltage; and

a multiplexer configured to multiplex said first output and said second output to a third output.

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20. (AMENDED) An apparatus comprising:

a first stage comprising (A) a first device comprising (i) a first gate configured to receive an input voltage ranging from greater than a first supply voltage to at least a second supply voltage, (ii) a first drain configured to receive said first supply voltage, and (iii) a first source coupled to an output, and (B) a first resistive element having (i) a first side coupled to said first source and (ii) a second side configured to receive said second supply voltage; and

a second stage comprising (A) a second device comprising (i) a second gate configured to receive said input voltage, (ii) a second drain configured to receive said second supply voltage, and (iii) a second source coupled to said output, and (B) a second resistive element having a first side coupled to said second source and a second side configured to receive said first supply voltage, wherein said apparatus is arranged such that a maximum voltage drop

(continued)

across each gate oxide of said first device and said second device does not exceed a difference between said first supply voltage and said second supply voltage.